School of Computer Science

60-265-01 Computer Architecture and Digital Design

Fall 2010

Midterm Examination # 2

Wednesday, November 17, 2010

Student Name: _____ _____
First Name Family Name

Student ID Number: _____

Duration of examination: 75 minutes

1. Answer all questions on this examination paper in the space provided.
2. This is a closed-book examination – no notes or books, calculators or electronic computing or storage devices may be used.
3. Do not copy from or communicate with other students in any way. All questions will be answered only by the attending proctors.
4. All students must remain seated during the last 5 minutes of the examination unless instructed otherwise by the proctors.
5. The examination must be surrendered immediately when the instructor or proctor announces the end of the test period.
6. Each student must sign the examination sign-out list before leaving the classroom. Failure to sign out may invalidate the student's examination.

Total mark obtained: _____

Maximum mark: 54

Question 1. [12 marks]
Answer all parts of this question.

A. State briefly what is wrong, if anything, with the following register transfer statement. **[1 mark]**

```
Q  :  R1 = R2 , R1 = R1
```

You cannot enable both the LOADs at the same time.

B. State briefly what is wrong, if anything, with the following register transfer statement. **[1 mark]**

```
Q  :  R1 = R2 , R2 = R1 + 1
```

Nothing is wrong.

C. Register R1 contains the 4-bit binary value 1001. Assuming that R1 is operated on using the RTL statement below so that the value in R1 is changed to 1110 after the operation is performed. Determine the binary value that must be in a register R2, plus determine the logic operation ***op*** to be performed in order to obtain the R1 output stated. **[2 marks]**

```
R1 = R1 op R2
```

1001 XOR 0111 = 1110

Op is XOR, R2 = 0111 (Check for alternatives)

D. Starting from an initial value of R = 10011101, determine the sequence of binary values in R after each operation in the sequence: (1) an arithmetic shift-right, (2) followed by a logical shift-right, (3) followed by a logical shift-left, and (4) followed, finally, by a circular shift-left. Show all your work. **[4 marks]**

Ashr(10011101) leads to 11001110
Lshr(11001110) leads to 01100111
Lshl(01100111) leads to 11001110
Cshl(11001110) leads to 10011101 Final answer

Question 1 (continued)

E. Assume that a memory unit contains 2K words with each word consisting of 16 bits. How many address lines are needed to access each word in the memory unit? **[1 mark]**

2K = 2 x 2^{10} = 2^{11}, hence 11 bits are needed for address lines.

F. Assume that a memory unit contains 2M words with each word consisting of 32 bits. How many 8-bit bytes can be stored in the memory unit? **[1 mark]**

2 x 2^{20} x 4 = 2^{23} bytes

G. Assuming that the stored value in a T-flipflop is Q before enabling the circuit, what is the value stored after applying the input T=1 with clock enabled? **[1 mark]**

Value stored is Q' (Q complement)

H. How many flip-flops will be complemented in a 12-bit binary counter to reach the next count after **101101111111**? **[1 mark]**

Binary counters represent unsigned binary values. Thus, adding 1 to the initial value yields the value:

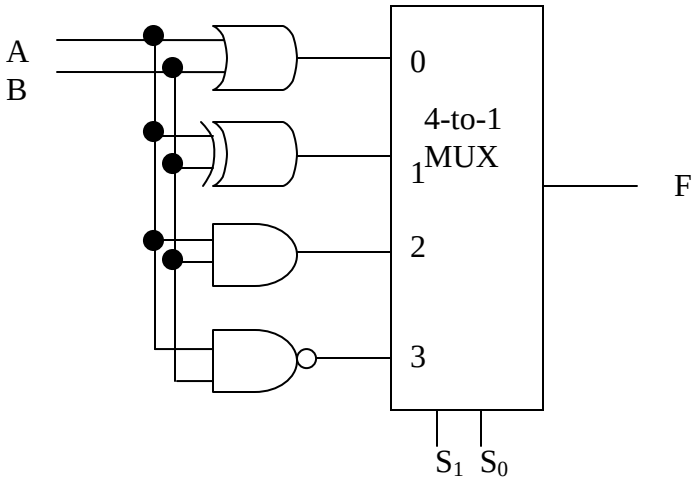
```
  101101111111
+ 000000000001
  101110000000
```

As seen above, **8 flip-flops must be complemented**.

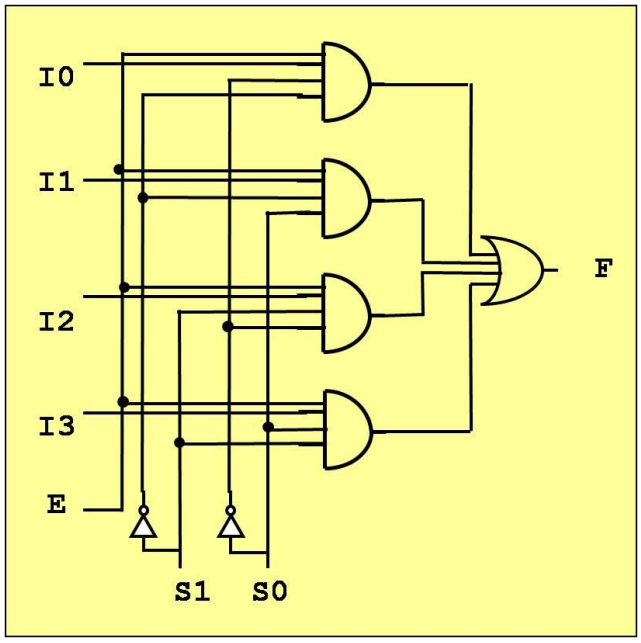
Question 2. [20 marks] Answer all parts of this question.

A. Design a digital circuit that performs one of the four logic operations of A OR B, A XOR B, A AND B and A NAND B. The choice of operation is determined using selection inputs to a multiplexer. Show the block diagram assuming two 1-bit inputs A and B. The output from the circuit is F. **[5 marks]**

The circuit block diagram is shown below. Note how each logic gate is applied to A and B, in parallel, but the MUX serves to select one of these to pass through to the output F.



B. Design and draw the logic circuit for a 4-to-1 line multiplexer with enable input using fundamental logic gates. Label your circuit diagram. **[5 marks]**



C. Design and draw the logic circuit for a 4-to-2 line encoder using fundamental logic gates. Label your circuit diagram. **[5 marks]**

The truth table is:

I0	I1	I2	I3	D1	D0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Thus, it follows that:

$$D0 = I0'.I1.I2'.I3' + I0'.I1'.I2'.I3$$

$$D1 = I0'.I1'.I2.I3' + I0'.I1'.I2'.I3$$

The circuit diagram follows straightforwardly as two 4-input AND gates and 1 2-input OR gate for each output line D_k.

If it is assumed that the inputs are mutually exclusive, the answer could be

$$D0 = I1 + I3$$
$$D1 = I2 + I3$$

D. Draw a complete circuit diagram for a 2-bit register with LOAD enable input. Initially, the stored values in the register flip flops are **Q0** and **Q1**. When LOAD is enabled, the applied inputs are **I0** and **I1**, which then replace **Q0** and **Q1**, respectively. When LOAD is disabled, the register simply refreshes its stored values. You may use any suitable type of flipflop. **[5 marks]**

If we start with D-flipflops it makes the task more straightforward. Assume that the LOAD input is labeled LD.

The state equations for the flipflops are:

$$Q0^+ = Q0.LD' + I0.LD$$

$$Q1^+ = Q1.LD' + I1.LD$$

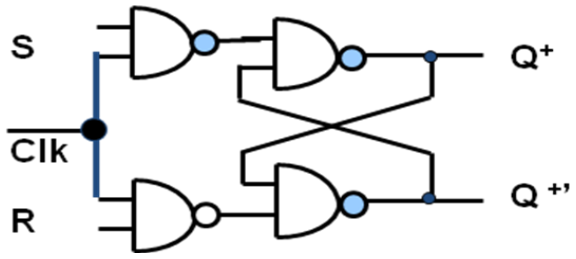
These are easily drawn as a circuit digram.

Question 3. [9 marks]
Answer all parts of this question that deals with flipflops.

Part A. State the complete truth table for a SR-latch using the symbol Q to denote the initial stored value, and Q+ to denote the final stored value after applying the SR inputs? Indicate any forbidden states, if they exist. **[3 marks]**

S	R	Q	Q+	
0	0	Q	Q	
0	1	Q	0	
1	0	Q	1	
1	1	Q	Q	(forbidden)

Part B. Draw the complete circuit diagram for a clock enabled SR-latch using only NAND gates. **[3 marks]**



Note that even inverter gates can be expressed using NAND gates!

Part C. State both the characteristic table and the characteristic equation for a standard JK-flipflop. Use Q to denote the initially stored value, and Q+ to denote the stored value after applying the JK inputs. **[3 marks]**

Characteristic Table

J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	Q′

Characteristic equation

$Q^+ = JQ' + K'Q$

Question 4. [13 marks]
Answer all parts of this question that deals with decoders.

Part A. Design a 2-to-4 (2x4) line decoder with enable input. State the complete truth table and draw the corresponding circuit diagram. **[4 marks]**

The truth table is:

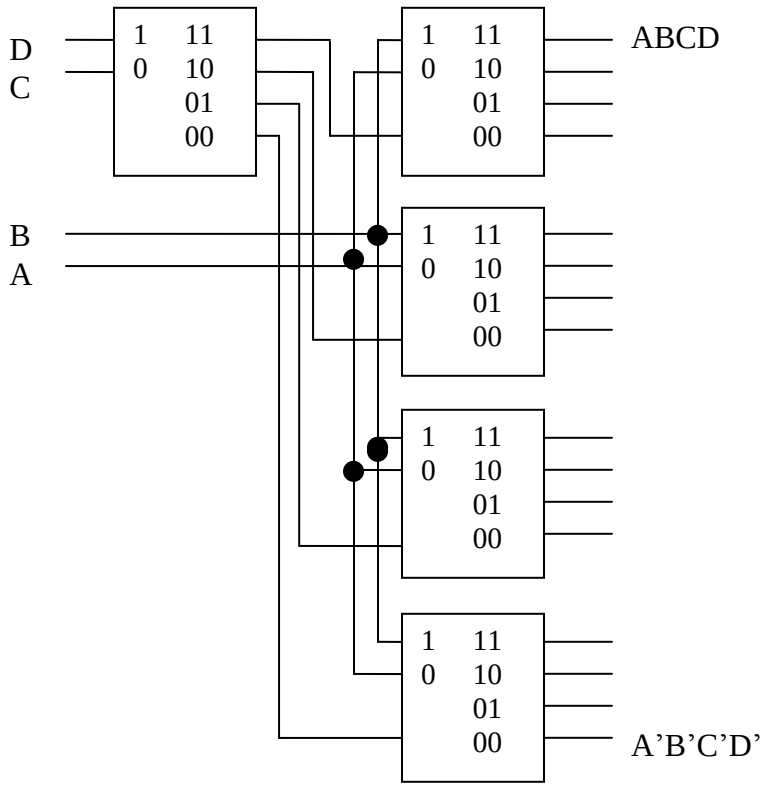
I1	I0	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Thus, it follows that:

$D0 = I0'.I1'$ $D1 = I0.I1'$ $D2 = I0'.I1$ $D3 = I0.I1$

The circuit diagram follows straightforwardly as <u>four</u> 2-input AND gates for each output line D_k.

Part B. Construct a **4-to-16** line decoder using <u>five</u> **2-to-4** decoders with enable inputs. The inputs to the circuit are **A**, **B**, **C**,and **D**. Label the **<u>first and last</u>** decoder outputs as minterm expressions. Use block diagrams <u>only</u>. **[4 marks]**



Trace this circuit carefully. The order of the outputs of this circuit is not from 00 to 15.

Question 4 (continued)

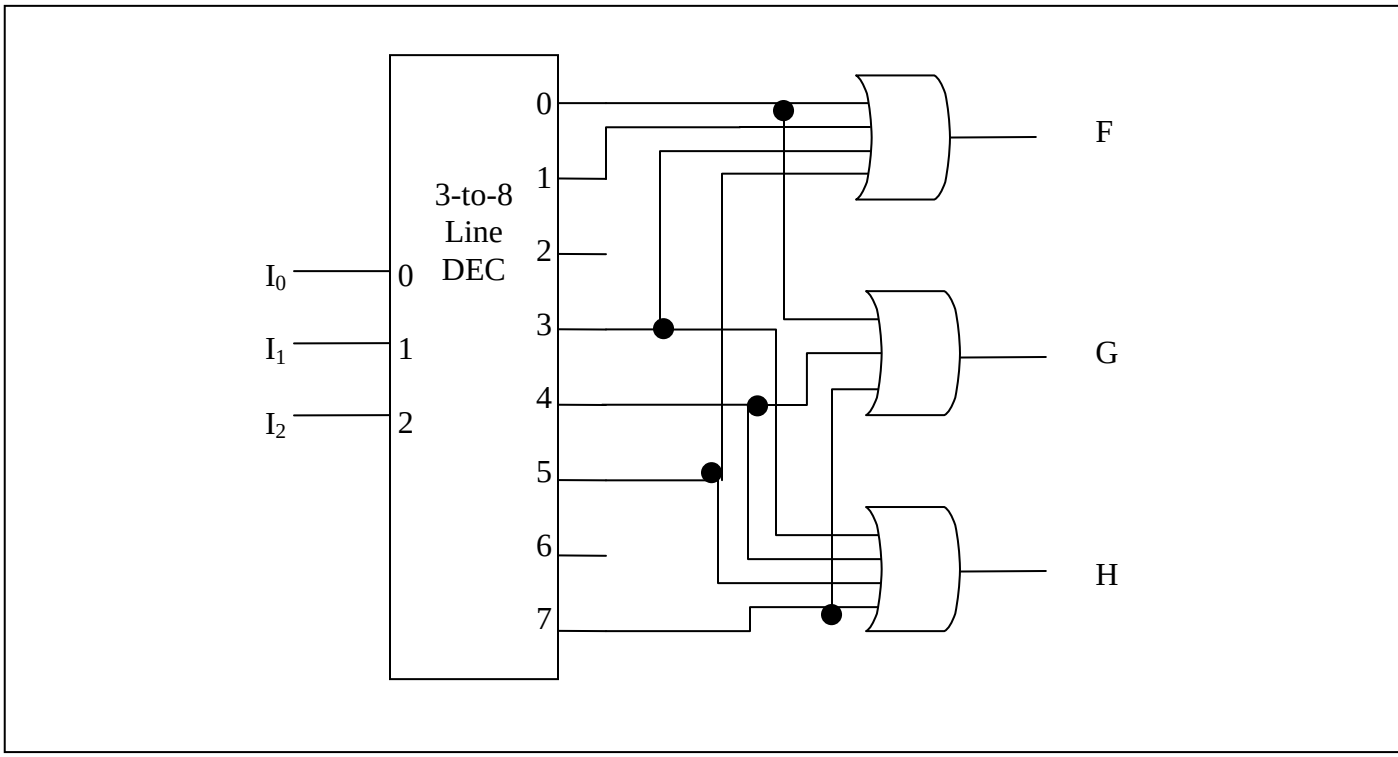
Part C. A 3-to-8 line decoder has been provided in the diagram below with inputs labelled 0..2 and outputs labelled 0..7. It is not necessary to define the internal circuit (treat it as a "black box"). It is required to obtain a full circuit that accepts inputs I_0, I_1 and I_2 and produces the three outputs F, G and H defined as follows:

$$F(I_0,I_1,I_2) = \sum m(0,1,3,5)$$

$$G(I_0,I_1,I_2) = \sum m(0,4,7)$$

$$H(I_0,I_1,I_2) = \prod M(0,1,2,6)$$

Complete the circuit defined algebraically above by inserting appropriate gates and connections in the diagram below. NOTE: the inputs MUST be connected directly to the decoder, and the decoder outputs MUST be connected to the control logic into each of the specified outputs F, G and H. **[5 marks]**



Note that since H is expressed in Maxterm notation, it must be modified to Minterm notation to use the decoder outputs directly.

This page contains various definitions and information provided freely for each student to use for the examination, if required. You may detach this page.

Boolean Postulates:

P0: Existence: There exist at least two elements x,y in B such that $x \neq y$

P1: Closure: For every x,y in B there exist two combinational operators + and . where x+y is in B and x.y is in B

P2: Identity: There exist identity elements 0,1 in B relative to the operations + and ., such that for every x in B: 0+x = x+0 = x and 1.x = x.1 = x.

P3: Commutativity: The operations + and . are commutative for all x,y in B: x+y = y+x and x.y = y.x

P4: Distributivity: Each operation + and . is distributive over the other; that is, for all x,y,z in B: x.(y+z) = x.y+x.Z and x+(y.z) = (x+y).(x+z)

P5: Complementation: For every element x in B there exists an element ~x, called the complement of x, satisfying: x+~x = 1 and x.~x = 0