School of Computer Science
60-265-01 Fall 2012

Midterm Examination # 2

Tuesday, November 13, 2012

Student Name: _____ _____
First Name **Family Name**

Student ID Number: _____

Marker Copy

Duration of examination: 75 minutes

1. Answer all questions on this examination paper in the space provided.
2. This is a closed-book examination – no notes or books or electronic computing or storage devices may be used.
3. Do not copy from other students or communicate in any way. All questions will be answered only by the attending proctors.
4. All students must remain seated during the last 5 minutes of the examination.
5. The examination must be surrendered immediately when the instructor, or attending proctor, announces the end of the test period.
6. Each student must sign the examination list before leaving the classroom.

Total mark obtained: _____
Maximum mark: 51

Question 1. [10 marks]

Answer all parts of this question.

A. Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 215_{10} in binary (base-2) representation. [1 mark]

215 converts to: 128 + 64 + 16 + 4 + 2 + 1

In 12-bit binary notation: 000011010111

B. Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 215_{10} in radix-7 (base-7) representation. [1 mark]

215 converts to: 4*49 + 2*7 + 5

In 12-bit binary coded base-7 notation: 000100010101

C. Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 215 in binary coded decimal (BCD). [1 mark]

In 12-bit binary coded decimal notation: 001000010101

D. To the nearest power of 10, state the approximate number of bytes represented by a Terabyte. [1 mark]

Answer: 1 Terabyte = 2^{40} bytes = $(2^{10})^4 = (1024)^4 \sim (10^3)^4 = 10^{12}$

E. Assume that registers R1 and R2 are 6-bit registers. Further, assume that R1 contains the 6-bit binary value 011010, and the operation R1 xor R2 obtains the 6-bit binary output value 100001. State the 6-bit binary value in R2 that will provide the correct output.

Answer: We are trying to solve for: 011010 xor bbbbbb = 100001. Since A xor B gives 1 if A and B are not equal, and 0 if they are equal, it is straightforward to obtain the R2 bits, namely R2 = 111011. An interesting property of xor is that A xor (A xor B) gives the result B. Try this out on this question: 011010 xor 100001 = 111011 = B. This technique is commonly used in computer graphics games for "sprites" and other effects.

F. Assume that a memory unit contains 4K words with each word consisting of 16 bits. How many address lines are needed to access each word in the memory unit? **[1 mark]**

Answer: $4K = 4 \times 2^{10} = 2^{12}$, hence 12 bits are needed for address lines.

G. How many flip-flops will be complemented in a 12-bit binary counter to reach the next count after **001101011111**? **[1 mark]**

Binary counters represent unsigned binary values. Thus, adding 1 to the initial value yields the value:

```
  001101011111
+ 000000000001
  001101100000
```

As seen above, **6 flip-flops must be complemented**.

H. Assuming that the stored value in a T-flipflop is Q before enabling the circuit, what is the value stored after applying the input T=1 with the circuit enabled? **[1 mark]**

Answer: Value stored is Q' (Q complement)

I. Assume that a digital computer has a common bus system for 16 registers. Each register has 32 bits stored in flipflops. How many selection inputs must there be in the address bus multiplexer? [1 mark]

Answer: 4 selection inputs must be provided.

J. Assume that a digital computer has a common bus system for 16 registers. Each register has 32 bits stored in flipflops. How many multiplexers are there in the data bus? [1 mark]

There must be 1 MUX for each bit, hence 32 MUXes are needed in the bus.

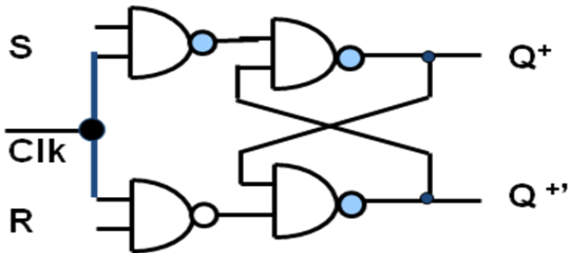
Question 2. [17 marks]

Part A. State the complete truth table for a SR-latch using the symbol Q to denote the initial stored value, and Q+ to denote the final stored value after applying the SR inputs? Indicate any forbidden states, if they exist. **[3 marks]**

S	R	Q	Q+	
0	0	Q	Q	
0	1	Q	0	
1	0	Q	1	
1	1	Q	Q	(forbidden)

Part B. Draw the complete circuit diagram for a clock enabled SR-latch using only NAND gates. **[3 marks]**

From lecture notes:



Part C. Draw the complete circuit diagram for a JK flipflop with enable input, using fundamental logic gates. Label your diagram. **[3 marks]**

See lecture notes.

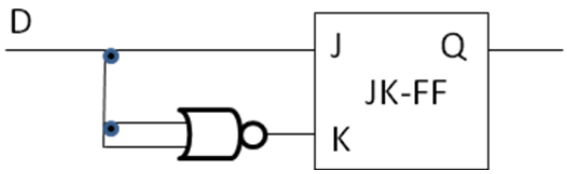
Part D. State the characteristic equation for a standard JK-flipflop. Also, state the complete characteristic table for the JK-flipflop using **Q** to denote the initially stored value, and $\mathbf{Q}^+$ to denote the stored value after applying the JK inputs. **[3 marks]**

Characteristic Table Characteristic Equation

J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q′

$$Q^+ = JQ' + K'Q$$

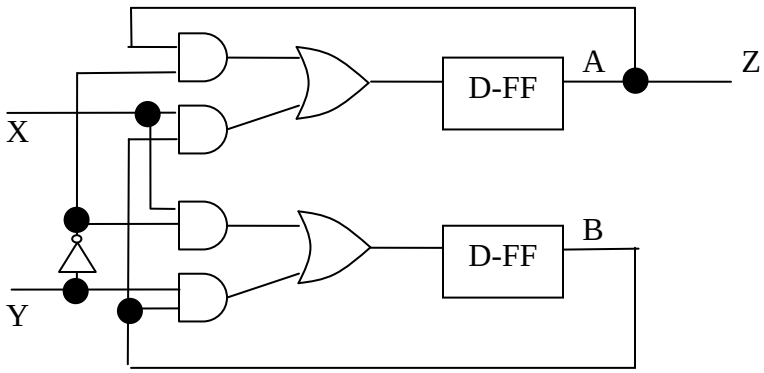
Part E. Design and draw an equivalent circuit for a D-flipflop using only a JK-flipflop and NOR gate(s). Use a block diagram for the JK-flipflop. **[2 marks]**



Part F. A sequential circuit has two D flip-flops, called A and B, two inputs called X and Y, and one output called Z. The flip-flop input equations and the circuit output are as follows:

$$D_A = Y' A + X B \qquad D_B = X Y' + Y B \qquad Z = A$$

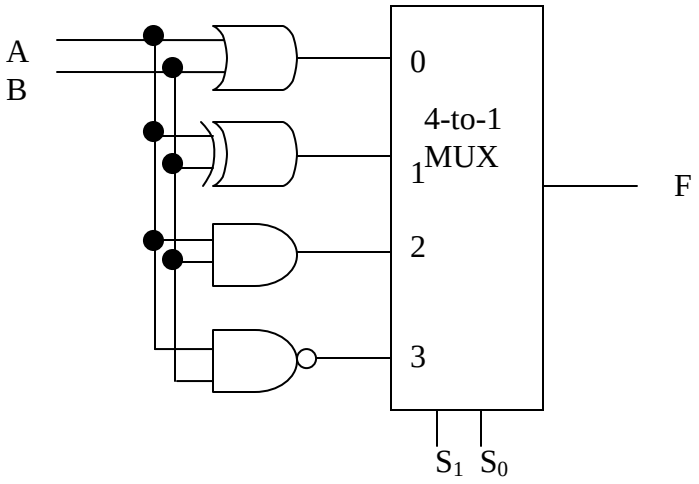
Draw the logic diagram of the circuit. **[3 marks]**



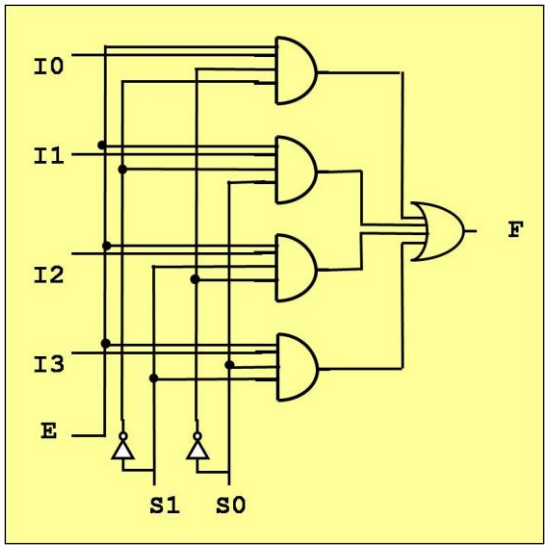
Question 3. [8 marks]

A. Design a digital circuit that performs one of the four logic operations: A OR B, A XOR B, A AND B and A NAND B. The choice of operation is determined using selection inputs to a multiplexer. Show the fully labeled block diagram assuming two 1-bit inputs A and B. The output from the circuit is F. **[4 marks]**

The circuit block diagram is shown below. Note how each logic gate is applied to A and B, in parallel, but the MUX selects only one of these to pass through to the output F.



B. Design and draw the logic circuit for a 4-to-1 line multiplexer with enable input using fundamental logic gates. Label your circuit diagram. **[4 marks]**



Question 4. [8 marks]

Design the complete circuit that accepts input from a 4-bit register R, and outputs a 3-bit result F where the result is the number of bits in R with value 1. For example, if R=0000 the output F=000, if R=1010 the output F=010 (ie. 2), while if R=1111 the output F=100 (ie. 4).

Derive the Boolean expressions for each output bit of F = {F0,F1,F2} where F0 is the low-order bit and F2 is the high-order bit. Use truth-tables and Karnaugh maps to find your results.

ANSWER: The truth table for the complete circuit is:

R3	R2	R1	R0	F2	F1	F0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	0	1	0
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	1	0	0

Thus: F2 is very simple as it is solely represented by the minterm F2 = R0 R1 R2 R3. The Karnaugh maps for F1 and F2 are shown below:

F0 R0 R1 \ R2 R3	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

F1 R0 R1 \ R2 R3	00	01	11	10
00			1	
01		1	1	1
11	1	1		1
10		1	1	1

F0 consists of 8 minterms in an SOP expression (or 8 maxterms in a POS expression) and cannot be simplified further. The terms can be read directly from the table above.

F1 can be simplified to 6 product terms (or 6 sum terms), each with 3 literals, to form an SOP (or POS) expression. There is no unique answer for this, but expressions can be read by inspection from the table above.

Question 5. [8 marks]

Consider the following RTL statements (with comments):

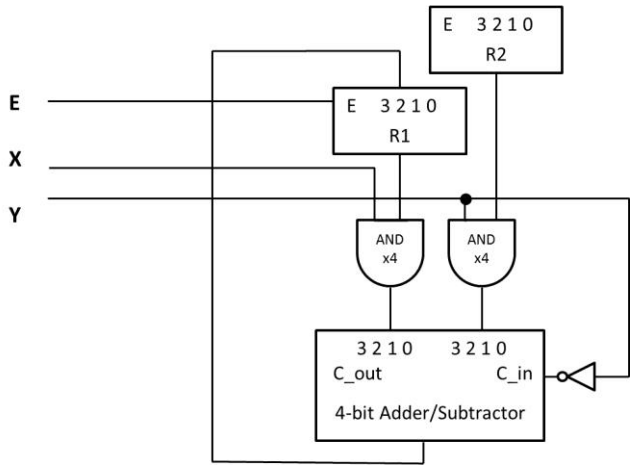
```
E'      : R1 ← R1          Refresh R1
E X'Y   : R1 ← R2          Load R2 into R1
E X Y   : R1 ← R1 + R2     Add R2 to R1, store in R1
E X Y'  : R1 ← R1 + 1      Increment R1, store in R1
E X'Y'  : R1 ← 1           Set R1 to 1 in all bits
```

Design and draw a complete, fully labeled circuit diagram for the above group of five RTL statements, assuming Enable input E, control inputs X and Y, and assume that R1 and R2 are each 4 bit registers that refresh automatically when the Enable is off (ie. 0). You should use block diagrams of circuit elements in your answer. Define the function of each such block diagram unless it is a fundamental gate and state all assumptions.

Answer:

For this question it is useful to assume a 4-bit Adder/Subtractor with Carry-in bit. This module was defined in lecture notes and can be used to perform the R1+R2 addition, but it can also be used to form the sum R1=R2+0 by simply ANDing the R1 inputs with 0 before the Adder/Subtractor, and finally R1=R1+1 can be dealt with by ANDing the R2 inputs with 0 before the Adder/Subtractor and inputting a 1 as the Carry-in bit to the Adder/Subtractor.

Students should carefully trace the circuit diagram shown below to understand how it works. The ANDx4 module performs ANDing between X (Y) and each separate bit of R1 (R2), so that the output is either all 0's (if X=0) or R1 (if X=1). Note that the Carry-in to the Adder/Subtractor is 0 when Y=1 and 1 when Y=0 (for the R1=R1+1 and R1=1 operations).



This page contains various definitions and information provided freely for each student to use for the examination, if required. You may detach this page.

Boolean Postulates:

P0: Existence: There exist at least two elements x,y in B such that $x \neq y$

P1: Closure: For every x,y in B there exist two combinational operators + and . where x+y is in B and x.y is in B

P2: Identity: There exist identity elements 0,1 in B relative to the operations + and ., such that for every x in B: 0+x = x+0 = x and 1.x = x.1 = x.

P3: Commutativity: The operations + and . are commutative for all x,y in B: x+y = y+x and x.y = y.x

P4: Distributivity: Each operation + and . is distributive over the other; that is, for all x,y,z in B: x.(y+z) = x.y+x.Z and x+(y.z) = (x+y).(x+z)

P5: Complementation: For every element x in B there exists an element ~x, called the complement of x, satisfying: x+~x = 1 and x.~x = 0