

Exercise 4 – Combinational Circuit Design

Question 1. Circuit Inspection [4 marks]

Assume that a combinational circuit with 4 inputs {A,B,C,D} and 2 outputs {F,G} has been defined as follows, using a hierarchical approach with interim line values {T1,T2,T3,T4}:

$$T1 = B'C \quad T2 = A'B \quad T3 = A + T1 \quad T4 = D \text{ xor } T2' \quad F = T3 + T4 \quad G = D' + T2$$

- (a) List the truth table for all possible inputs {A,B,C,D} and also the interim values of {T1,T2,T3,T4} and finally, {F,G}

| A | B | C | D | T1 | T2 | T3 | T4 | F | G |
|---|---|---|---|----|----|----|----|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

- (b) Plot the truth tables, using maps, to determine if the circuit expressions for F and G can be simplified further.

| F | | CD | | | |
|----|----|----|----|----|----|
| | | 00 | 01 | 11 | 10 |
| AB | 00 | 1 | 0 | 1 | 1 |
| | 01 | 0 | 1 | 1 | 0 |
| | 11 | 1 | 1 | 1 | 1 |
| | 10 | 1 | 1 | 1 | 1 |

$$F = A + B'D' + BD + CD = A + B \text{ xnor } D + CD \quad \text{6 literals}$$

$$\text{From above: } F = T3 + T4 = A + B'C + D \text{ xor } (A'B)' = A + B'C + D(A'B) + D'(A+B') \quad \text{7 literals}$$

Question 2. Circuit Design [3 marks]

A. Design a combinational circuit with 3 inputs and 1 output.

- a. The output is 1 when the unsigned binary value of the input is less than 3, otherwise it is 0.

The truth table is given as follows:

| X2 | X1 | X0 | F |
|----|----|----|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

The SOP expression is: $F = X_0'X_1'X_2' + X_0 X_1'X_2' + X_0 X_1 X_2' = X_1'X_2' + X_0 X_2'$

- b. The output is 1 when the binary value is even, otherwise it is 0.

The truth table is given as follows:

| X2 | X1 | X0 | F |
|----|----|----|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The SOP expression is: $F = X_0'X_1'X_2' + X_0'X_1 X_2' + X_0'X_1'X_2 + X_0'X_1 X_2 = X_0'$

Note that this result is obvious if one considers that the definition of an even number is when the low order bit is $X_0=0$, or $X_0'=1$, regardless of what the higher order bits are.

- B. Design a combinational circuit with 3 inputs {X,Y,Z} and 3 outputs {A,B,C}. When the unsigned binary value of the inputs is 0,1,2 or 3, the binary output is one greater than the input value. When the unsigned binary value of the inputs is 4,5,6 or 7, the binary output is 2 less than the input value.

The truth table is given as follows:

| X | Y | Z | A | B | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

The SOP expressions are:

$$A = X'YZ + XYZ' + XYZ = \mathbf{XY + YZ}$$

$$B = X'Y'Z + X'YZ' + XY'Z' + XY'Z = \mathbf{X'Y'Z + X'YZ' + XY'}$$

$$C = X'Y'Z' + X'YZ' + XY'Z + XYZ = \mathbf{X'Z' + XZ}$$

- C. When two 4-bit signed binary values are added, it is possible that an arithmetic overflow occurs. For example, the largest signed binary number is the bit-string 0111. If 1 is added to this, it leads to an overflow condition. Design the combinational circuit expression for an output Overflow bit V, where V=0 denotes no overflow, while V=1 denotes an overflow has occurred. Test your solution carefully to demonstrate that it works.

Note that an overflow cannot occur if one number is positive while the other is negative (consider examples to satisfy yourself that this is the case). Thus, overflow can only happen if both inputs are either positive, or negative – the overall sign of the inputs is obtained by considering the high order bit H. Thus, if H=0 the number is positive (actually, non-negative, including 0) while if H=1 the number is negative. Referring to the high order bits of the inputs as A_H and B_H , and the output sum high order bit as S_H , the overflow condition is arrived at if and only if S_H is different than A_H (or B_H) when $A_H = B_H$. Thus,

$$V = A_H B_H S'_H + A'_H B'_H S_H$$

Question 3. A 4-bit to 8-bit Multiplier Circuit [3 marks]

Design a combinational multiplier circuit that takes two 4-bit inputs, {A} and {B} and produces an 8-bit output {P}, where the value $P = A \times B$; that is, the product of A with B. Assume that A and B are unsigned binary numbers. In your circuit you must use 4-bit binary full adders (as derived in the lectures, or referenced in the textbook) arranged in stages, along with other circuitry, to achieve the final 8-bit product output {P}.

In addition to the above, briefly describe what steps are required to modify the circuit designed to meet the objectives stated above, such that arbitrary 2's complement 4-bit binary numbers are input to the (modified) multiplier circuit, and the output is an 8-bit product that is properly stated as a 2's complement binary number, including the proper handling of the sign.

One approach to multiplying non-negative input values is fully outlined, in detail, in the textbook. Students should read the section of the textbook that deals with this problem.

To deal with arbitrary 2's complement input values, one approach is to detect the sign of each input (by checking the high order bit) and form the 2's complement to obtain the non-negative value when the input value itself is a negative number. One then performs the multiplication as above for non-negative numbers. As a final step, the sign of the output value is determined by taking the XOR of the input high order bits. If these bits are different (ie. one is negative while the other is non-negative) then the result is negative (or zero); thus, one final 2's complement operation can be performed on the output to obtain the final circuit output answer. No such 2's complement "correction" is required if the input high order bits are the same (ie. since the product of two negatives is a positive, as is the product of two positives, or non-negatives).

Additional Assigned Reading and Self-study Exercises:

Review and attempt all problems 4.1 to 4.65 at the end of Chapter 4 in the textbook; you may omit the questions that deal with HDL unless you are specifically interested. It is not required that students submit their work, nor will it be evaluated. However, examination questions may be based on these problems, so it is worthwhile to complete this work.

Evaluation:

- A. All Laboratory Exercises must be completed and submitted for grading by the following Laboratory session, unless otherwise prescribed by the Instructor.
- B. Students are evaluated on all stated requirements.
- C. It is mandatory that students complete their own work and must be able to justify their answers when asked to do so by teaching staff.