60-265 Computer Architecture I: Digital Design Fall 2012

Exercise 5 – Combinational Circuit Design II

Question 1. Decoders/Encoders [5 marks]

(a) Draw the logic diagram of a 2-to-4 line decoder using: (i) NOR gates only, and (ii) NAND gates only. Include an enable input.
(b) Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable, and a 2-to-4 line decoder. Use block diagrams for the components.
(c) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

E = X'YZ' + XZ F = XY'Z' + X'Y G = X'Y'Z' + XY

(d) Design a four-input priority encoder with inputs as in Table 4.8 of the textbook, but with input D0 having the highest priority and input D3 the lowest priority. (NOTE: Read the textbook.)

All of the above questions are straightforward exercises. Any student who has difficulties with any of these should see the Instructor, or GA's, or raise questions in the lab. The (d) part is discussed in detail in the textbook.

Question 2. Multiplexers [4 marks]

A. Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.

This problem was straightforward and almost all students obtained a correct solution. Of the 16 inputs, 8 of them are attached to the inputs of one 8x1 multiplexer, while the remaining 8 are attached to the other 8x1 multiplexer. Of the required 4 selector inputs, 3 of them are attached in parallel to both of the selector inputs for the 2 8x1 multiplexers. The remaining selector input is attached to the selector input of the 2x1 multiplexer. The two outputs from the 2 8x1 multiplexers are inputted to the input lines of the 2x1 multiplexer so that the final output is the initial input selected by all four selector inputs.

B. Implement the following Boolean function with a 4x1 multiplexer and external gates.

F(A,B,C,D) = SUM m(1,2,5,7,8,10,11,13,15)

Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D. These values are obtained by expressing F and a function of C and D for each of the four cases when AB = 00, 01, 10, and 11. These functions may have to be implemented with external gates.

ANSWER: The four expressions for F are given below for each AB case.

F(0,0,C,D) = SUM m(1,2)

F(0,1,C,D) = SUM m(5,7)

F(1,0,C,D) = SUM m(8,10,11)

F(1,1,C,D) = SUM m(13,15)

Each of the functions above can be expressed as a simple two-stage SOP circuit constructed using only C and D inputs (since A and B are defined in each case, simplification results). The outputs from each of these circuits is inputted to the 4x1 multiplexer using A,B as selector inputs to select the appropriate F function as output.

C. Implement a full adder with two 4x1 multiplexers.

Referring to lecture notes, the expressions for the full adder outputs are:

S = Cin A' B' + Cin' A B' + Cin' A' B + Cin A B

Cout = (Cin Cin') A' B' + Cin A B' + Cin A' B + Cin' A B

Note that the first term in the expression for Cout above is just 0. With the expressions in these forms, one notes immediately that by using AB as the selector inputs of the two 4x1 multiplexers, one can form the output S by attaching the Cin to the AB=00, 11 inputs and Cin' (complement) to the AB=01,10 inputs of one of the multiplexers. The Cout output is obtained by attaching the Cin input to the AB=01,10,11 inputs of the other multiplexer. For this multiplexer, both Cin and Cin' are ANDed to form a 0 result which is then inputted to the AB=00 input.

Question 3. Circuit Design [1 mark]

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise. Do not use a ripple comparator approach.

ANSWER: We note that for two bits A_k and B_k, applying the XNOR operator gives a result of (A_k XNOR B_k) = 1 if and only if $A_k = B_k$. Thus, since all four corresponding bits must be equal and all equalities must apply at the same time, it follows that the comparator circuit output E (for equality) is expressed by ANDing all four XNOR bit expressions, hence:

$E = (A_0 \text{ XNOR } B_0)\ (A_1 \text{ XNOR } B_1)\ (A_2 \text{ XNOR } B_2)\ (A_3 \text{ XNOR } B_3)$

Additional Assigned Reading and Self-study Exercises:

Review and attempt all problems 4.1 to 4.65 at the end of Chapter 4 in the textbook; you may omit the questions that deal with HDL unless you are specifically interested. It is not required that students submit their work, nor will it be evaluated. However, examination questions may be based on these problems, so it is worthwhile to

complete this work. Students should also be reading Chapter 5 on sequential circuits. Next week's lab will involve questions on sequential circuits.

Evaluation:

A. All Laboratory Exercises must be completed and submitted for grading by the following Laboratory session, unless otherwise prescribed by the Instructor.
B. Students are evaluated on all stated requirements.
C. It is mandatory that students complete their own work and must be able to justify their answers when asked to do so by teaching staff.