60-265 Computer Architecture I: Digital Design Fall 2012

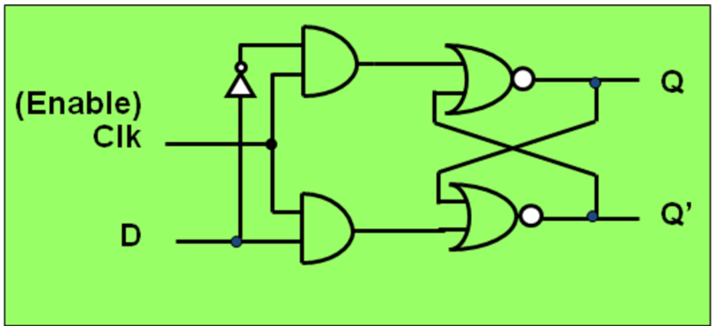
Exercise 6 – Sequential Circuit Design

Question 1. D Latch [3 marks]

The D latch (or flip-flop) was constructed in the lecture notes. Consider the following three ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.

(a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.

The diagram below is taken directly from lecture notes. Note the single inverter from the D input to the upper AND gate. The SR latch is implemented using NOR gates.



(b) Use NOR gates for all four gates. Inverters may be needed.

The trick in this part is to convert AND gates to NOR gates, and the inverter to a NOR gate. The latter is straightforward using the algebraic transformation:

X’ = (X+X)’, using idempotency, so that NOT X = NOT (X OR X) = X NOR X

It also follow that:

XY = (XY)’’ = ((XY)’)’ using double complementation, then = (X’ + Y’)’ = X’ NOR Y’ using de Morgan’s theorem, and with the above relation for X’ = X NOR X,

XY = X’ NOR Y’ = (X NOR X) NOR (Y NOR Y)

These relations can be implemented as logic gates to transform the diagram shown in Part (a).

(c) Use four NAND gates only (without an inverter).

It is useful to know how to express each gate in terms of other gates. In this case, we need to transform NOR gates, from Part (b) to NAND gates.

For the specific case of the inverter, we derive:

X’ = (XX)’ = X NAND X using idempotency.

We also require:

$$(X + Y)' = X'Y' = (X'Y')'' = ((X'Y')' (X'Y')')' = (X' \text{ NAND } Y') \text{ NAND } (X' \text{ NAND } Y')$$

In the rightmost expression above, you should substitute $X' = X$ NAND X (and similarly for Y') to complete the transformation. These relations can be implemented as logic gates to transform the diagram shown in Part (a), and the expressions derived in Part (c).

Question 2. JK Flip-flops [5 marks]

A. Construct a JK flip-flop using a D flip-flop, a 2-to-1 multiplexer, and an inverter (if required).

To see how to approach this, consider the table below:

Q	**J**	**K**	**Q^+**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	1	0	1
1	0	1	0
1	1	1	0

The rows have been sorted by Q=0 and Q=1. In the case of Q=0 we note that the value to be stored in the D flipflop, namely Q^+, is given by the value of the input J. In the case of Q=1, the value to be stored in the D flipflop is given by K'.

Thus, by connecting the Q output from the D flipflop into the selector input of the 2x1 MUX, and directing the J input to the 0 channel and K' to the 1 channel of the 2x1 MUX inputs, and finally connecting the output from the 2x1 MUX to the input of the D flipflop, we have constructed the circuit as specified.

B. Show that the characteristic equation for the complement output of a JK flip-flop is:

$$Q'(t+1) = J'Q' + KQ$$

This can be proven using the *method of perfect induction* (also known as a truth table), hence:

J	**K**	**$Q^{+'}$**
0	0	Q' (Refresh)
0	1	Q'+Q=1 (Set)
1	0	0+0=0 (Reset, or Clear)
1	1	Q (Complement)

The table above was derived directly from the characteristic equation and covers all input cases, hence is proven.

C. Related to the JK flip-flop is the PN flip-flop. A PN flip-flop has four operations: Clear to 0 (PN=00), no change (refresh, PN=01), complement (PN=10), and Set to 1 (PN=11).

a. Tabulate the characteristic table.

P	**N**	**Q^{+}**	**Q^{+}’**
0	0	0	1
0	1	Q	Q’
1	0	Q’	Q
1	1	1	0

b. Derive the characteristic equation.

Q^{+} = PQ’ + NQ $\qquad\qquad$ Q^{+}’ = P’Q’ + N’Q

c. Show how the PN flip-flop can be converted to a D flip-flop.

P	**N**	**J**	**K**	**Q^{+}**	**Q^{+}’**
0	0	0	1	0	1
0	1	0	0	Q	Q’
1	0	1	1	Q’	Q
1	1	1	0	1	0

The table above shows the output values for corresponding PN and JK inputs (the JK inputs in the blue columns are to be associated with their corresponding PN inputs). From the table it is clear, by inspection that the relationships are:

J = P $\quad$ K = N’

Thus, by inverting the K value before inputting to the N input, and applying J directly to the P input, one transforms the PN flipflop to the JK flipflop.

Question 3. Circuit Design [2 marks]

Design and draw a sequential circuit with two JK flip-flops called A and B. there are two inputs to the circuit, E and F. If E=0, the circuit remains in its initial state, regardless of what value F has. When E=1 and F=1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 and back to 00 again, repeating the transitions so long as the circuit is asynchronously enabled. When E=1 and F=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 and back to 11 again, repeating the transitions while the circuit is enabled. Treat the A flip-flop as the low-order bit and B as the high-order bit.

Consider a specific sequence, as in the table below, with the increment (E=F=1) case on the left and the decrement (E=1, F=0) case on the right. The X (Y) label denotes the higher (lower) order bit:

X	Y	X+	Y+		X	Y	X-	Y-
0	0	0	1		0	0	1	1
0	1	1	0		0	1	0	0
1	0	1	1		1	0	0	1
1	1	0	0		1	1	1	0

We note that in both cases Y is complemented, that is $Y_{after} = Y_{previous}'$, for every step in the sequence if E=1, regardless of the value of F.

For F=1, following the left table,

$X+ = X'Y + XY' = X \text{ xor } Y$

For F=0, following the right table,

$X- = X'Y' + XY = X \text{ xnor } Y$

Thus, we can conclude that, in general, for the X bit (the high order bit), the following expressions apply when the circuit is enabled, E=1, using the subscript *post* to denote the values of X and Y after the right hand side operations have been performed:

$Y_{post} = Y'$ $X_{post} = F(X \text{ xor } Y) + F'(X \text{ xnor } Y)$

We can now relate the above considerations towards the JK flipflops themselves. We use the labels J_A,K_A,J_B,K_B to refer to the respective inputs of the A and B JK-flipflops, and Q_{Aprev}, Q_{Bprev} to the respective outputs at a given time. We also assume, for simplicity, that each of the A and B JK-flipflops are equipped with Enable inputs so that we can turn them on/off using E=1/0. That simplifies dealing with the remaining parts of the circuit by connecting the E input directly to each of the Enable inputs of A and B.

From above it is clear that $Y= Q_{Aprev}$, therefore we need to apply the inputs $J_A=K_A=1$ to force the A JK-flipflop to perform the complement operation. Review the operation of the JK flipflop in previous questions to better understand why we do this, if it is not immediately clear to you. We can ensure that both inputs are equal to 1 by recalling that the complementation should only occur when the circuit is enabled. Thus, we connect E to both J_A and K_A, and so long as E=1, the complementation is continuously performed. If E=0, then $J_A=K_A=0$ and the flip flop simply refreshes itself.

In the final step, from above, we note that $X= Q_{Bprev}$, and recall that $Y= Q_{Aprev}$. It follows that, including the E input, we derive the *posterior* (or post) value of X:

$$Q_{Bpost} = EF(Q_{Bprev} \text{ xor } Q_{Aprev}) + EF'(Q_{Bprev} \text{ xnor } Q_{Aprev})$$

Note that for JK flipflops, when JK=10, the value 1 is stored (Set), while if JK=01, the value 0 is stored (Reset). In the case of the B JK-flipflop, we apply:

$J_B = Q_{Bpost}$ $K_B = Q'_{Bpost}$

This circuit ensures that the final updated value in the B JK-flipflop is $Q_B^+ = Q_{Bpost}$.

A SUBLETY:

There is one more issue to consider and it has to do with timing control. Obviously, the time it takes for the complementation of the A flipflop to occur, is less than the time it would take for the 2-stage combinational circuit module that must be executed before providing JK control inputs to the B flipflop.

Earlier in the course we introduced a so-called *buffer* element that has two inputs and one output. We described it as a capacitor device that accepts a wire input Z, but then holds the value so long as a control input C=0 is applied. When the control input C=1, the value Z is permitted to pass through the gate to the output. Thus, it is a suitable delay gate.

We can use this type of gate to solve the timing problem mentioned above between the A and B flipflops. We leave this as an advanced topic, however.

Additional Assigned Reading and Self-study Exercises:

Review and attempt all problems 5.1 to 5.60 at the end of Chapter 5 in the textbook; you may omit the questions that deal with HDL unless you are specifically interested. It is not required that students submit their work, nor will it be evaluated. However, examination questions may be based on these problems, so it is worthwhile to complete this work. Students should also be reading Chapter 6 on Register and Counter circuits. Next week's lab will involve questions on registers and counters.

Evaluation:

A. All Laboratory Exercises must be completed and submitted for grading by the following Laboratory session, unless otherwise prescribed by the Instructor.
B. Students are evaluated on all stated requirements.
C. It is mandatory that students complete their own work and must be able to justify their answers when asked to do so by teaching staff.