60-265 Computer Architecture I: Digital Design Fall 2012

Exercise 7 – Register Transfer Level (RTL) Logic

Question 1. Register Transfer I [1 mark]

Show the block diagram of the hardware that implements the following register transfer statement:

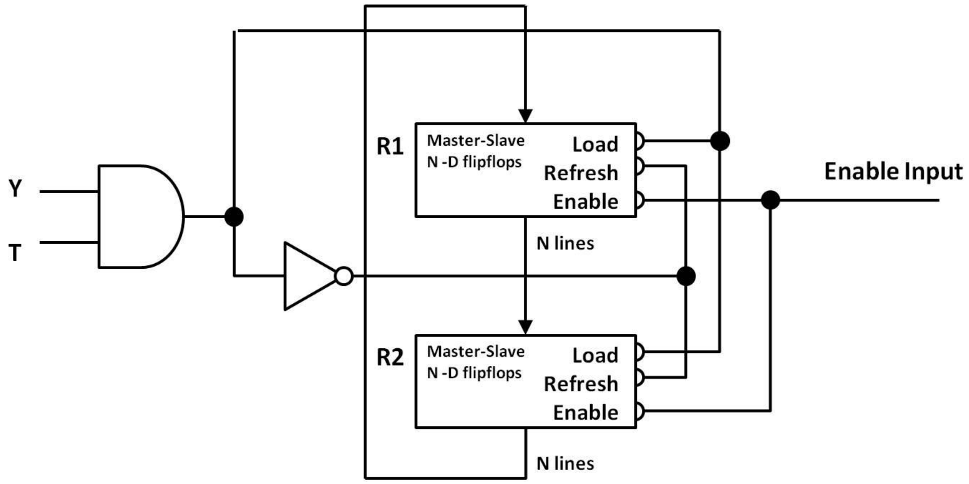
`Y. T : R2 = R1 , R1 = R2` (NOTE: All micro-operations are done in parallel.)

This circuit swaps the contents of R1 and R2 when both Y and T inputs are true (ie. both equal to 1). Represent the registers as block modules with both data and control inputs, including Enable, Load and Refresh. State what kind of flip-flop circuit should be used to implement the swap between R1 and R2.

ANSWER: Parallel transfers between registers may be carried out straightforwardly when one recalls that the outputs of one register are being used as the inputs to the other, and vice versa, but that these are controlled through a logic control interface.

The timing logic on resolving the final outputs of the register flip-flops is usually handled using Master-Slave flip-flops. Thus, when T=1 and Y=1 the Load is enabled; however, at the next step, T=0, so regardless of Y, the AND gate output is 0, so the Refresh is enabled and the register flip-flops stabilize.

Thus, this could be drawn as something like below, assuming master-slave D flip-flops:



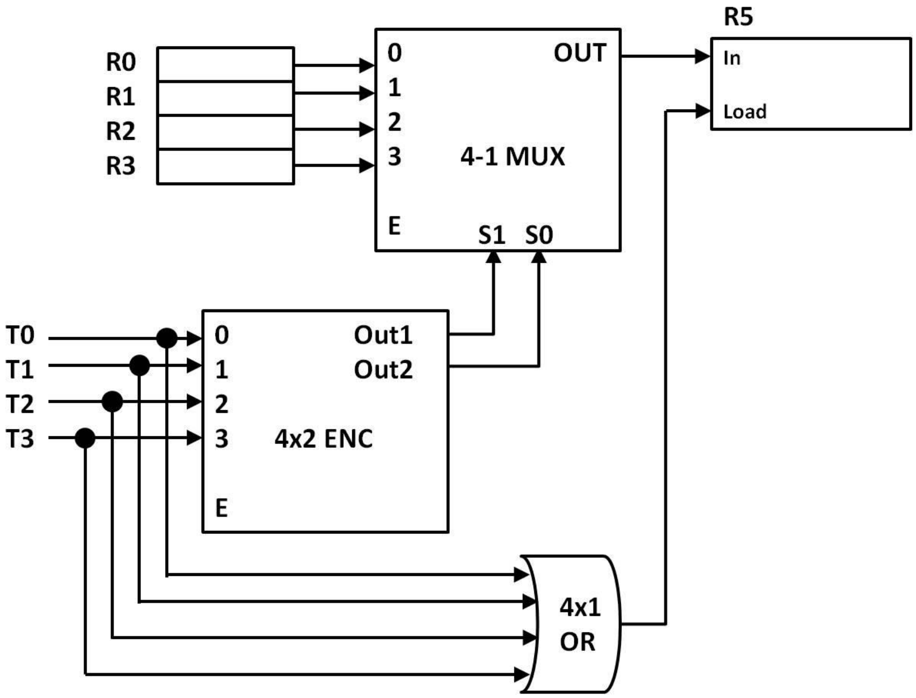
Question 2. Register Transfer II [2 mark]

The outputs of four registers, R0, R1, R2 and R3, are connected through 4-to-1 line multiplexers to the inputs of a fifth register R5. Each register is eight bits long. The required transfers are dictated by four timing variables (T0 through T3) in a timed sequence as follows:

```
T0 : R5 = R0
T1 : R5 = R1
T2 : R5 = R2
T3 : R5 = R3
```

The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load control input of register R5.

ANSWER: One possible approach is illustrated below.



Question 3. Register Transfer III [2 marks]

Represent the following conditional control statement expressed in pseudo-code by two register transfer statements with control conditions.

If (P = 1) then (R1 = R2) else If (Q = 1) then (R1 = R3)

ANSWER:

```
  P : R1 = R2
P'Q : R1 = R3
```

NOTE: Students often misinterpret the meaning of RTL. RTL statements should not be thought of as a sequence of programming operations, or statements. Thus, ALL of the statements together refer to hardware circuits that are constantly connected to other circuits and electrical (ie. voltage) supplies. The specific circuits are enabled only when enabling voltage signals are applied; hence, when the enabling, or control, conditions are evaluated to 1, the circuit is enabled. This point is emphasized in the second RTL statement where P' must be indicated as part of the condition (ANDed with the value of Q).

Question 4. Register Transfer IV [3 marks]

State what is wrong (ie. incorrect) with each of the following register transfer statements.

```
a. X.T :  R0 = ~R0 ,  R1 = 0       Nothing wrong

b. Y.T :  R2 = R3,  R2 = R4        Cannot do both at same time

c. Z.T :  R5 = R6,  R5 = R5 + 1    Cannot do both at same time

d.  R0 :  R0 = R0 + 1              Nothing wrong
```

Question 5. Micro-operation Sequencing [2 marks]

The 8-bit registers AR, BR, CR and DR initially have the following values:

```
AR = 11110010,  BR = 11111111,  CR = 10111001,  DR = 11101010
```

Determine the 8-bit values in each register after the complete execution of the following sequence of micro-operations.

```
AR = AR + BR                  Add BR to AR storing answer in AR
CR = CR ^ DR , BR = BR + 1    AND DR to CR, INC BR
AR = AR - CR                  Subtract CR from AR
```

```
AR + BR =    11110010
           + 11111111
          (1)11110001
AR = 11110001

CR ^ DR =    10111001
           ^ 11101010
             10101000
CR = 10101000

BR + 1 =     00000000
BR = 00000000

AR - CR  =  11110001 - 10101000
         =  11110001 + ~(10101000) + 1
         =  11110001 + 01010111 + 1
         =  11110001
          + 01010111
          + 00000001
            01001001
AR = 01001001
```

Evaluation:

A. All Laboratory Exercises must be completed and submitted for grading by the following Laboratory session, unless otherwise prescribed by the Instructor.
B. Students are evaluated on all stated requirements.
C. It is mandatory that students complete their own work and must be able to justify their answers when asked to do so by teaching staff.