Exercise 8 – Instruction Cycle - Timing Logic

Question 1. Direct Addressing Load Cycle [7 marks]

The timing cycle for the Load Accumulator (LDA) instruction, using **direct access** to memory M is provided below. The notation used is the same as in the lecture notes. Note that the register transfer level (RTL) micro-operations listed are also consistent with the lecture notation (and attributed to M. Mano).

T0 : AR = PC, SC = SC + 1
T1 : DR = M[AR], IR = M[AR], PC = PC + 1, SC = SC + 1
T2 : {D7,D6,...,D1,D0} = DEC(IR(12-14)), I = IR(15), AR = IR(0-11), SC = SC + 1
I' D2 T3 : AC = M[AR], SC = 0

The registers PC, AR, IR, SC and AC are the same as defined in the lecture notes, while the I and DECoder outputs Dx and timing decoder outputs Tx are also the same as defined in the lecture notes.

Draw a complete and well-labeled block diagram for this circuit, showing how the various connections must be made to control the timing sequence for the LDA instruction cycle.

Hint: Note that the entire circuit, and each individual element within the circuit (such as individual registers) are always ready to perform their function and are just waiting for an enable condition to be fulfilled so they can proceed. Thus, it is useful to isolate the various components of the LDA circuit and determine what conditions must be fulfilled in order to direct enabling of sub-circuit elements.

ANSWER:
The block diagram provided below is considerably more detailed than expected for this lab; however, it is sufficiently detailed to illustrate many aspects of circuit design. Note that the diagram shown still lacks many features, including proper handling of the bus logics for both RAM and CPU registers.

First, we recast the RTL statements above so that the focus of control is changed to isolate each individual hardware operation such as Load, Increment, Enable and so on. Study this logic carefully before going on to the diagram.

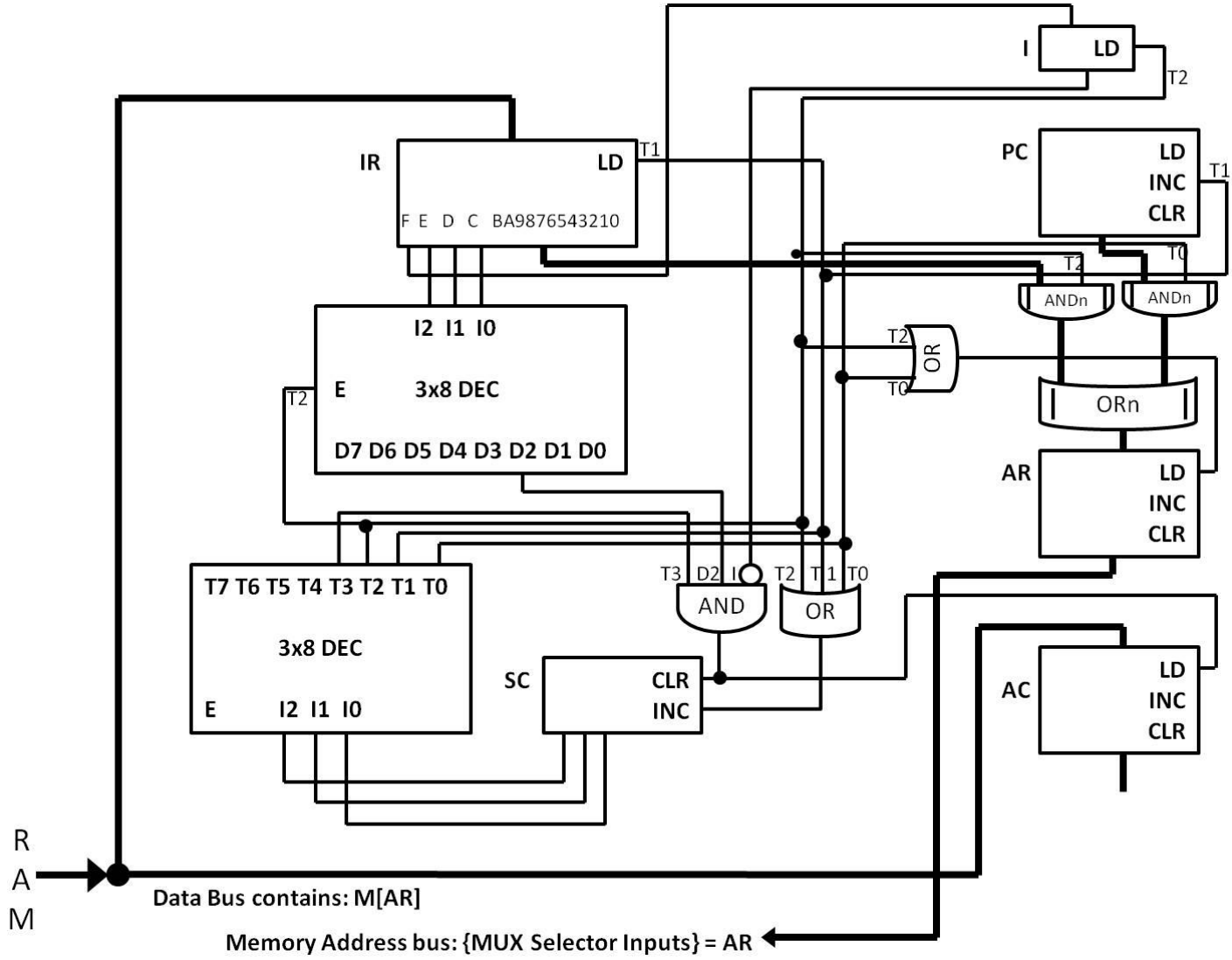
Condition	**Statement**	**Comment**
T0 + T2	**: AR = (PC ^ T0) ∨ (IR(0-11) ^ T2)**	Enable Load AR using T0, T2 with multibit AND/OR to select input
T0+T1+T2	**: SC = SC + 1**	Increment SC is T0, T1, T2 time steps
T1	**: IR = M[AR]**	Enable IR Load
T1	**: PC = PC + 1**	Enable PC Increment
T2	**: {D7,D6,...,D1,D0} = DEC(IR(12-14))**	Enable Decoder
T2	**: I = IR(15)**	Enable I Load

I' D2 T3 : AC = M[AR] Apply AR to Address Bus MUX, Enable AC Load

I' D2 T3 : SC = 0 Enable SC Clear

In the diagram, a few blocks have been introduced that are straightforward. There is a block called ANDn that is meant to describe a set of n-AND gates, each with input T (a timing variable) and Rk (the k'th register bit). Similarly, there is a block called ORn with similar definition.

The thinner lines are intended to represent carrier wires with a single bit signal (voltage value). The thicker lines are intended to convey multiple bit buses carrying several bits between source and destination locations, including registers and the memory address and data buses.
The circuit diagram follows.



Question 2. Indirect Addressing Load Cycle [3 marks]

The timing cycle for the Load Accumulator (LDA) instruction, using **indirect access** to memory M is provided below. The notation used is the same as in the lecture notes. Note that the register transfer language and microoperations listed are also consistent with Mano's notation.

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  T0 : AR = PC, SC = SC + 1
  T1 : DR = M[AR], IR = M[AR], PC = PC + 1, SC = SC + 1
  T2 : {D7,D6,...,D1,D0} = DEC( IR(12-14) ), I = IR(15), AR = IR(0-11), SC = SC + 1
I D2 T3 : DR = M[AR], SC = SC + 1
I D2 T4 : AR = DR(0-11), SC = SC + 1
I D2 T5 : AC = M[AR], SC = 0
```

The registers PC, AR, IR, DR, SC and AC are the same as defined by Mano (and lecture notes), while the I and DECoder outputs Dx and timing decoder outputs Tx are also the same as defined by Mano.

Based on the block diagram for **Question 1** above, draw a block diagram for the different aspects of this circuit that perform the extra memory fetch and indicate whether there should be any changes to the direct addressing LDA. Also, show how the various connections must be made between your answer to this question and the diagram of Question 1 to control the timing cycle of the indirect addressing mode of the LDA instruction.

ANSWER:
Extending the diagram provided in the first part of this exercise is left for students.

Begin by accounting for the extra RTL statements introduced by the indirect addressing mode, with I=IR(15)=1, and the addition and/or extension of more AND and OR gates. Also featured in this part is the DR register. This can be incorporated in the diagram in Question 8.1 first. Once it has been incorporated, it is straightforward to draw the logic control parts to enable its Load operation.

FINAL COMMENT:
Once you have a good starting circuit for basic instruction control, you can see more easily how additional instructions can be added. With each instruction type goes a new set of control issues that must be distinguished from other control logics. Usually, these design problems require studying the combinational interfaces in the control logic problem. This exercise is a modest first step towards that bigger problem.

Evaluation:

A. All Laboratory Exercises must be completed and submitted for grading by the following Laboratory session, unless otherwise prescribed by the Instructor.
B. Students are evaluated on all stated requirements.
C. It is mandatory that students complete their own work and must be able to justify their answers when asked to do so by teaching staff.