60-265 Computer Architecture I: Digital Design Fall 2012

Exercise 9 – Machine Language Program Execution

Question 1. Program I [3 marks]

In the table below, ADR refers to memory addresses, while Contents refers to the value stored at the memory address location. Start the program execution with PC = 100. Note that ADR and Contents are expressed in hexadecimal.

ADR	Contents
100	2104
101	1105
102	3106
103	7001
104	1106
105	FFF8
106	0000

A = 1106
B = FFF8
SUM = 0000
SUM= A+B

ADR	Content	Mnemonic	RTL	PC	AR	IR	AC	DR	I	E
100	2104	LDA A	DR= M[AR] AC= DR	101	104	2104	1106	1106	0	0
101	1105	ADD B	DR= M[AR] AC=AC+DR	102	105	1105	10FE	FFF8	0	0
102	3106	STA SUM	DR=AC M[AR]=DR	103	106	3106	10FE	10FE	0	0
103	7001	HLT	Disable all circuits							
104	1106	First Op (A)								
105	FFF8	Second Op (B)								
106	0000	Store SUM								

Memory	
104	1106
105	FFF8
106	0000
Initial	

Memory	
104	1106
105	FFF8
106	10FE
Final	

Question 2. Program II [3 marks]

In the table below, ADR refers to memory addresses, while Contents refers to the value stored at the memory address location. Start the program execution with PC = 100. Note that ADR and Contents are expressed in hexadecimal.

ADR	Contents
100	1109
101	7200
102	3109
103	210B
104	110A
105	310B
106	6109
107	4103
108	7001
109	0005
10A	0002
10B	0000

A = 0005
B = 0002
SUM = 0000
A = ~A /*A=FFFA*/
While (A!=0)
{
SUM=SUM+B;
A=A+1;
}

ADR	Content	Mnemonic	RTL	PC	AR	IR	AC	DR	I	E
100	1109	ADD A	DR= M[AR] AC=AC+DR	101	109	1109	0005	0005	0	0
101	7200	CMA	AC=~AC	102	109	7200	FFFA	0005	0	0
102	3109	STA A	DR=AC M[AR]=DR	103	109	3109	FFFA	FFFA	0	0
103	210B	LDA SUM	DR= M[AR] AC=DR	104	10B	110B	0000	0000	0	0
104	110A	ADD B	DR= M[AR] AC=AC+DR	105	10A	110A	0002	0002	0	0
105	310B	STA SUM	DR=AC M[AR]=DR	106	10B	310B	0002	0002	0	0
106	6109	ISZ A	AR=IR(0-11) DR=M[AR] AC=DR AC=AC+1 DR=AC M[AR]=DR (AC=0): PC=PC+1	107	109	6109	~~FFFA~~ FFFB	~~FFFA~~ FFFB	0	0
107	4103	BUN 103	AR=IR (0-11) PC=AR	~~108~~ 103	103	4103	FFFB	FFFB	0	0

103	210B	LDA SUM	DR= M[AR] AC=DR	104	10B	110B	0002	0002	0	0
104	110A	ADD B	DR= M[AR] AC=AC+DR	105	10A	110A	0004	0002	0	0
105	310B	STA SUM	DR=AC M[AR]=DR	106	10B	310B	0004	0004	0	0

106	6109	ISZ A	// increment A if
			A=0 stop
				107	109	6109	~~FFFB~~
							FFFC
								~~FFFB~~
								FFFC
									0	0

107	4103	BUN 103	AR=IR (0-11) PC=AR	~~108~~ 103	103	4103	FFFC	FFFC	0	0
103	210B	LDA SUM	DR= M[AR] AC=DR	104	10B	110B	0004	0004	0	0
104	110A	ADD B	DR= M[AR] AC=AC+DR	105	10A	110A	0006	0002	0	0
105	310B	STA SUM	DR=AC M[AR]=DR	106	10B	310B	0006	0006	0	0

106	6109	ISZ A	// increment A if
			A=0 stop
				107	109	6109	~~FFFC~~
							FFFD
								~~FFFC~~
								FFFD
									0	0

107	4103	BUN 103	AR=IR (0-11) PC=AR	~~108~~ 103	103	4103	FFFD	FFFD	0	0
103	210B	LDA SUM	DR= M[AR] AC=DR	104	10B	110B	0006	0006	0	0
104	110A	ADD B	DR= M[AR] AC=AC+DR	105	10A	110A	0008	0002	0	0
105	310B	STA SUM	DR=AC M[AR]=DR	106	10B	310B	0008	0008	0	0

106	6109	ISZ A	// increment A if
			A=0 stop
				107	109	6109	~~FFFD~~
							FFFE
								~~FFFD~~
								FFFE
									0	0

107	4103	BUN 103	AR=IR (0-11) PC=AR	~~108~~ 103	103	4103	FFFE	FFFE	0	0
103	210B	LDA SUM	DR= M[AR] AC=DR	104	10B	110B	0008	0008	0	0
104	110A	ADD B	DR= M[AR] AC=AC+DR	105	10A	110A	000A	0002	0	0
105	310B	STA SUM	DR=AC M[AR]=DR	106	10B	310B	000A	000A	0	0

106	6109	ISZ A	// increment A if
			A=0 stop
				107	109	6109	~~FFFE~~
							FFFF
								~~FFFE~~
								FFFF
									0	0

107	4103	BUN 103	AR=IR (0-11) PC=AR	~~108~~ 103	103	4103	FFFF	FFFF	0	0
103	210B	LDA SUM	DR= M[AR] AC=DR	104	10B	110B	000A	000A	0	0
104	110A	ADD B	DR= M[AR] AC=AC+DR	105	10A	110A	000C	0002	0	0
105	310B	STA SUM	DR=AC M[AR]=DR	106	10B	310B	000C	000C	0	0

106	6109	ISZ A	// increment A if
			A=0 stop
				~~107~~
				108
					109	6109	~~FFFF~~
							0000
								~~FFFF~~
								0000
									0	1

108	7001	HLT	Disable all circuits							
109	0005	First Op (A)	A, DEC 5							

10A	0002	Second Op (B)	B, DEC 2	
10B	0000	Store (SUM)	SUM, DEC 0	

Memory	
109	0005
10A	0002
10B	0000
Initial	

Memory	
109	~~0005 , FFFA, FFFB, FFFC FFFD, FFFE, FFFF,~~ 0000
10A	FFF8
10B	~~0000, 0002, 0004, 0006 0008, 000A,~~ 000C

Memory	
109	0000
10A	0002
10B	000C
Final	

Question 3. Program III [4 marks]

In the table below, ADR refers to memory addresses, while Contents refers to the value stored at the memory address location. Start the program execution with PC = 100. Note that ADR and Contents are expressed in hexadecimal. Be very careful with this problem. In particular, if you find that there is an infinite loop, or any other problem that prevents completion of execution, state that in your answer.

ADR	Contents
100	2116
101	9117
102	3116
103	2117
104	6117
105	B117
106	7004
107	4100
108	7001
109	0005
10A	0002
10B	FFFF
10C	0101
10D	1010
10E	5106
10F	0000
110	0001
111	0002
112	0003
113	0004
114	0005
115	0000
116	0000
117	0110

ADR	Contents	Mnemonic	RTL	PC	AR	IR	AC	DR	I
100	2116	LDA 116	DR= M[AR] AC= DR	101	116	2116	0000	0000	0
101	9117	ADD 117	AR=IR(0-11) DR= M[AR] AR=DR(0-11) DR=M[AR]	102	~~117~~ 110	9117	0001	~~0110~~ 0001	1

			AC=AC+DR						
102	3116	STA 116	DR=AC M[AR]=DR	103	116	3116	0001	0001	0
103	2117	LDA 117	DR= M[AR] AC= DR	104	117	2117	0110	0110	0
104	6117	ISZ 117	AR=IR(0-11) DR=M[AR] AC=DR AC=AC+1 DR=AC M[AR]=DR (AC=0): PC=PC+1	105	117	6117	~~0110~~ 0111	~~0110~~ 0111	0
105	B117	STA 117	DR=AC M[AR]=DR	106	117	B117	0111	0111	1
106	7004	SZA	(AC=0):PC=PC+1	107					0
107	4100	BUN 100	AR=IR (0-11) PC=AR	~~108~~ 100	100	4100			0
100	2116	LDA 116	DR= M[AR] AC= DR	101	116	2116	0001	0001	0
101	9117	ADD 117	AR=IR(0-11) DR= M[AR] AR=DR(0-11) DR=M[AR] AC=AC+DR	102	~~117~~ 111	9117	0003	~~0111~~ 0002	1
102	3116	STA 116	DR=AC M[AR]=DR	103	116	3116	0003	0003	0
103	2117	LDA 117	DR= M[AR] AC= DR	104	117	2117	0111	0111	0
104	6117	ISZ 117	AR=IR(0-11) DR=M[AR] AC=DR AC=AC+1 DR=AC M[AR]=DR (AC=0): PC=PC+1	105	117	6117	~~0111~~ 0112	~~0111~~ 0112	0
105	**B**117	STA 117	DR=AC M[AR]=DR	106	117	B117	0112	0112	1
106	7004	SZA	(AC=0):PC=PC+1	107					0
107	4100	BUN 100	AR=IR (0-11) PC=AR	~~108~~ 100	100	4100			0
100	2116	LDA 116	DR= M[AR] AC= DR	101	116	2116	0000	0000	0
...									
108	7001	HLT	Disable all circuits						

Wrong end condition

109	0005
10A	0002
10B	FFFF

10C	0101
10D	1010
10E	5106
10F	0000
110	0001
111	0002
112	0003
113	0004
114	0005
115	0000
116	~~0000, 0001, 0003, 0006, 000A,~~ 000F
117	~~0110 , 0111, 0112, 0113 0114, 0115.~~ 0116(!!!)

Operation Codes and Mnemonics:

0 (8) AND	1 (9) ADD	2 (A) LDA	3 (B) STA
4 (C) BUN	5 (D) BSA	6 (E) ISZ	

7800 CLA	7400 CLE	7200 CMA	7100 CME
7080 CIR	7040 CIL	7020 INC	7010 SPA
7008 SNA	7004 SZA	7002 SZE	7001 HLT

F800 INP	F400 OUT	F200 SKI	F100 SKO
F080 ION	F040 IOF		

Evaluation:

A. All Laboratory Exercises must be completed and submitted for grading by the following Laboratory session, unless otherwise prescribed by the Instructor.
B. Students are evaluated on all stated requirements.
C. It is mandatory that students complete their own work and must be able to justify their answers when asked to do so by teaching staff.